One size DOESN'T fit all:

Honeywell TA-11 Roadmap Response

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Abstract

The NASA Flight Computing roadmap (TA11) is based upon the notion that a multi-core flight computer will lower Size, Weight, & Power for command & control functions. Honeywell's 50 years experience (NASA human, commercial & military satellites) & commercial & military aircraft & unmanned drones demonstrate LARGE differences in performance needs for vehicles. We have found four categories of flight computing: Fault Tolerant Human Rated Dynamic Control; Satellite bus attitude control; Satellite Payload processing; Robotics. A 2010 flight computer study to create a multi-core device to address the first three performance categories was completed showing a single device did not meet performance needs, but two designs using common building blocks did. Each has unique implementation & tipping points. We found a single design did not meet either system performance need and therefore would not be a preferred solution for NASA or any space organization. In addition to processing elements, Honeywell finds that implementation and standardization of a unified flight computing bus and improved Input/Output capability need to be developed. We recommend that NASA modify their roadmap to address each of these areas.

Honeywell Computer Chip Background

Honeywell has been providing radiation-hardened foundry services and ASIC products through its Plymouth organization since the early 1980s. These services started with a radiation-hardened version of a 1.2-micron bulk Complementary Metal-Oxide Semiconductor (CMOS) process, called Radiation Insensitive CMOS (RICMOS) III. This technology was used to fabricate the HR1000 ASIC family, the first five-chip GVSC processor (a space version of the MIL-STD-1750A), and the 16k and 64k SRAMs. Many of these products were used on the Trident and MILSTAR programs, among others. The radiation hardness capability includes Total Dose (TD) of 300 Krad to 1 Mrad, 1E-11 bit-errors/day Single Event Upsets (SEU), and Single-Event-Latchup immunity that easily meets the 2GLRV environments. Honeywell has maintained that level of radiation hardness capability throughout each process technology upgrade as shown in Figure 1.

The GVSC development was quickly followed by the RH32 (a R3000 radiation hardened knockoff). The progression continued with the development of the Honeywell radiation hardened 603e microprocessor. All of these developments are deployed in satellite systems and launch vehicles and are still in production today. As the processing needs of the today's systems continue to demand higher computation speeds, Honeywell started to develop the next generation of Honeywell space rated radiation-hardened device. In parallel to the development of the next generation satellite microprocessor, Honeywell was also trying to solve the computing power problem required to implement a Lunar Lander vehicle that could be launched by the 160 metric ton Ares V vehicle. The cost of parallel development of two microprocessors was recognized as challenging by the Honeywell management and thus directed the two teams to combine the processors into a single device that met the needs of both.

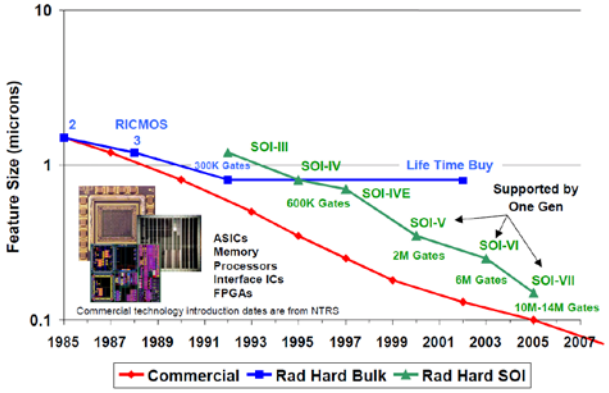

Figure 1 –*Honeywell's Radiation-hardened Technology Trend.* *Honeywell's radhard technology improvements continue to focus on increasing gate count and reducing feature size to provide the latest state-of-the-art, high-performance space products.*

Four Types of Systems

As part of the Honeywell, evaluation into the "single one size fits all chip" desired by the Honeywell management, the engineering staff started evaluating the work that needed to be performed by these devices and the figures of merit that would evaluate their performance. The first step in the analysis was creation of DoDAF artifacts describing the activity needed by each system was definition of the work. We identified three types of systems that Honeywell historically deployed:

- Fault Tolerant Human Rated Dynamic Control
- Satellite bus attitude control
- Satellite Payload processing

There is also a fourth category, Robotics, which could perform the work of one or all three of the categories identified above. The following figures (Figure 2a, Figure 2b, and Figure 2c) describe the boundary condition for each of the three systems.

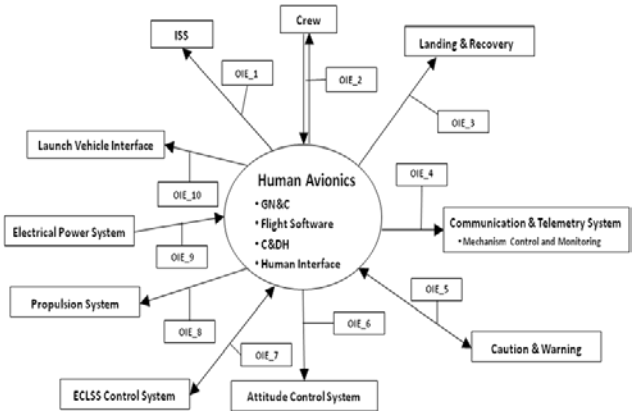

Figure 2a - Boundary Diagram for the Human Rated Dynamic Flight Computer

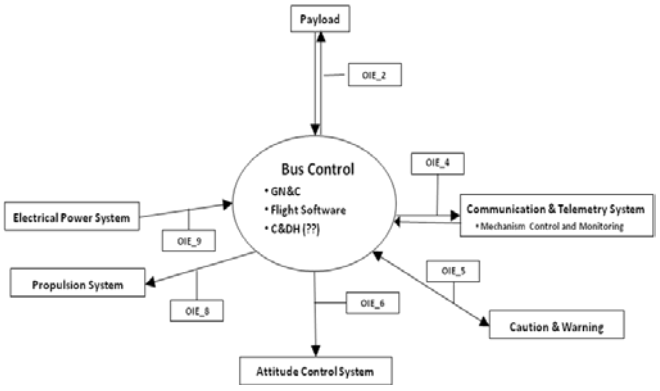

Figure 2b - Boundary Diagram for the Human Rated Dynamic Flight Computer

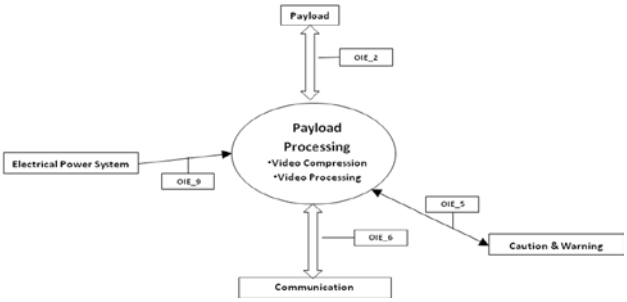

Figure 2c - Boundary Diagram for the Human Rated Dynamic Flight Computer

To solve this problem, Honeywell assigned a team of their most senior engineers from their space division (both the Clearwater campus and the Glendale campus), their advanced technology group, and the aircraft division. These engineers quickly noticed that there were also unique operational requirements for the three types of systems. The Fault Tolerant Human Rated Dynamic Control System required the lowest power because the mission was to go beyond low earth orbit with the following figure(s) of merit:

- Power (that must be generated; solar cells, fuel cells, etc.)
- Power (storage and management; batteries)
- Power (actually consumed by the flight computer)
- Power (represented by the weight required to reject the heat generated by the computer)
- Size
- Weight

To further emphasize the need for reduced SWaP for beyond LEO missions is the Altair requirements. Working with multiple prime contractors, the studies showed that the vehicle mass for the Altair was too heavy to be launched by the 160 metric tons Ares V without a 90% reduction in SWaP.

Since the Space Shuttle is able to complete its mission using the equivalent of an 80286 computer running at 12 Megahertz, the actual computational power needed is not the biggest issue. For the Orion program, the largest demand for computational power is to execute the abort logic and to create displays. The dynamic flight computer however, utilizes a large amount of program memory. The initial estimate of the Orion software was over two million source lines of code.

The other unique element of the dynamic flight control system is its requirement for instantaneous redundancy and synchronous operation. If a pyrotechnic must fire to protect the safety of the astronauts, the ability of the primary and secondary systems to fire in known deterministic time is essential.

The requirements for the satellite attitude control system were significantly different. While power was still an issue, these missions are limited to LEO, GEO, and HEO missions that do not pay the same penalty as beyond LEO missions. Because of the HEO environment, these missions require a higher radiation tolerance. Honeywell experience with these systems shows they are not highly memory intense; in fact, most systems are implemented in less than 8 Megabytes. These systems have higher computational requirements to close control loops for pointing systems and even current loops.

The third category is the payload processing. This area is where the NASA roadmap shined and clearly described the multi-core flight computer will lower Size, Weight, & Power for this type of intense data processing. Honeywell has been working on this area with concepts implemented and tested in its dependable multiprocessor.

It was clear from these diverse operational and functional requirements that a single architectural decomposition would not meet all three needs. Table 3 below shows the detailed trade requirements between the dynamic flight computer and the satellite computer attitude control system.

	NG-IMA (AIMS/EPIC/FC/FMS)	Human Space (Spacesuit..)	Non-Human Space
Radiation	**Rad-Tolerant** •Must be SEL immune and tolerant to SEU •SEU mitigated thru system redundancy •Radiation is atmospheric neutrons	**Rad-Tolerant** •Must be SEL immune and tolerant to SEU •SEU mitigated thru system redundancy	**Rad-Hard** •Must be implemented with rad-hard technology to survive natural and man-made radiation environments •Must be latch up immune •Proton immune and SEU LETth > 42 •SEU mitigated using design techniques
Core IP	**Hard Core** •DO-254 compliant •Soft IP could cost buckets of $$ to re-engineer and may not be feasible for a complex PPC core •Treat Hard IP same as a COTS device; multiple customers with physically identical cores •Simple soft IP processors that have supplier DO-254 artifacts are acceptable, like the NIOSII-SC which would be usable as a co-processor	**Hard or Soft Core** •No DO-254 requirements, can use either hard or soft core without restriction •However, soft core implementation may not yield optimal performance ,size, or power •May have future needs for DO-254 type design assurance, under investigation	**Soft Core** •No DO-254 requirements, can use either hard or soft core without restriction •Hard core IP would cost buckets of $$ to port to Honeywell's HX rad-hard ASIC technology •A soft core can be synthesized in Honeywell's HX rad-hard ASIC technology
Performance	**Internal eDRAM/Multicore** •Large sizes possible, 64-128MBytes •**NO** external devices needed •Only available on IBM's 45nm SOI process •Significantly **improves performance** •**Reduces power** over external devices •Reduces chip count, size, and PBA complexity •Dedicated co-processors for IO processing	**Internal eDRAM/Multicore** •Large sizes possible, 64-128MBytes, •**NO** external devices needed •Only available on IBM's 45nm SOI process •Significantly improves performance •**Reduces power** over external devices •**Reduces chip count, size**, and PBA complexity •Dedicated co-processors for IO processing	**Multicore/External memory** •Need low-latency high-bandwidth external memory interfaces (SRAM, SDRAM) •Need multiple lower speed (150 MHz) processor cores (rad-hard process limitation)
Competitive	•Low power, ~3W/device •Capable of Lockstep and Scalable-lock •Core frequency,1GHz minimum •Latest process, 45nm SOI •Latest generation core, IBM 476FP •Reasonable device cost, ~$150	•Low power, ~2W/device , <5W/SCP for Spacesuit to higher performance Orion VMC & Altair applications •Capable of Lockstep and Scalable-lock •Scalable Core frequency 1GHz minimum for Ares to low frequency for Spacesuit •Significant reuse of Orion VMC Core Software	•Higher Dhrystone performance than a RAD750 at 250 MHz •Higher Performance/Power ratio than competitors •Compatibility with existing PPC software development environments

Figure 3 – System on a Chip Trade study results. *The SoC trade study results are summarized with some of the key characteristics of Radiation, IP requirements, Performance, and Business reasons that justified to Honeywell management that one size did not fit all for the next generation processing chip Honeywell envisioned as needed for the next five years in the commercial aviation market and the space market.*

Type 1 Implementation

The implementation of the Fault Tolerant Human Rated Dynamic Control System (Type 1) system required moderate departure from current Honeywell architectures. Honeywell has advocated fail passive systems to meet the byzantine challenge for the past two decades. These systems have usually been implemented using self-checking pairs that check bit for bit at the instruction and memory level. With the entire system being on a single chip, the ability to do this and justify that a single piece of silicon did not have the ability to fail in a non-passive manner (e.g., babble) need to be changed. Figure 4 shows the top-level implementation of such a system.

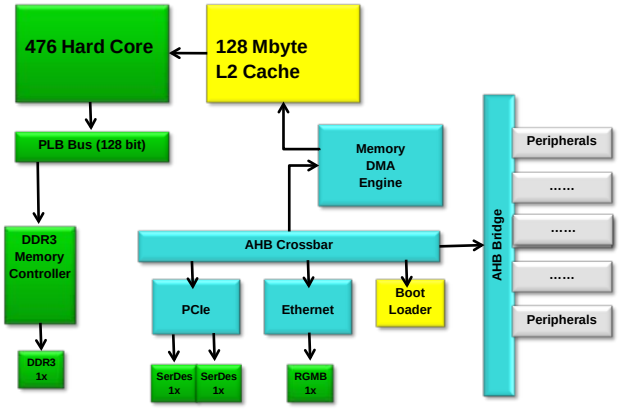

Figure 4 - System on a Chip Concept. *The Honeywell SoC concept utilizes existing TRL 6 (space) elements to meet the goal of 1/10 the size, weight, and power of the Orion SCP.*

The SoC concept proposed for the Type 1 system is backward compatible to both the 787 flight control module and the Orion self-checking pair (SCP). Figure 5a and Figure 5b show how the Honeywell concept SoC integrates into a block 2 Orion upgrade and Space Suite systems.

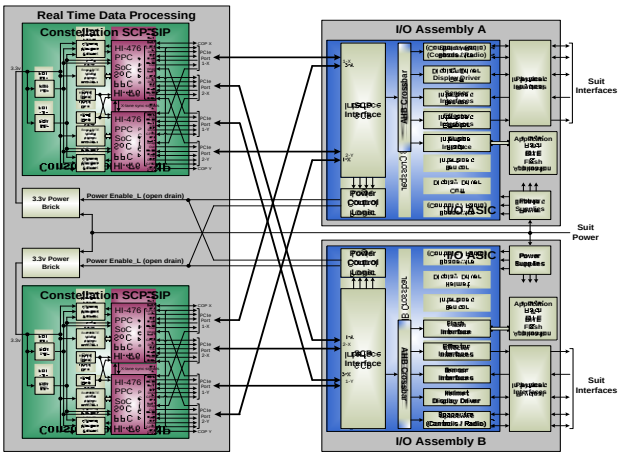

Figure 5a - Space Suit Implementation of SoC Concept.

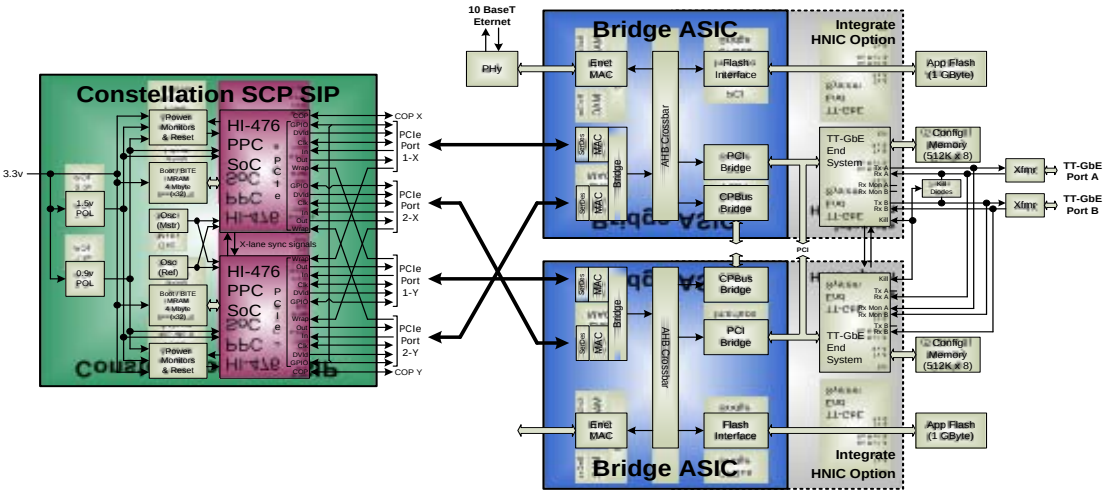

Figure 5b - Orion Implementation of SoC Concept.

The SoC concept implements the same open system as all prior Integrated Modular Avionic systems. Figure 6 shows the functional architecture and the implementation of partitions that are backward compatible with the current 787 flight control module and the Orion SCP.

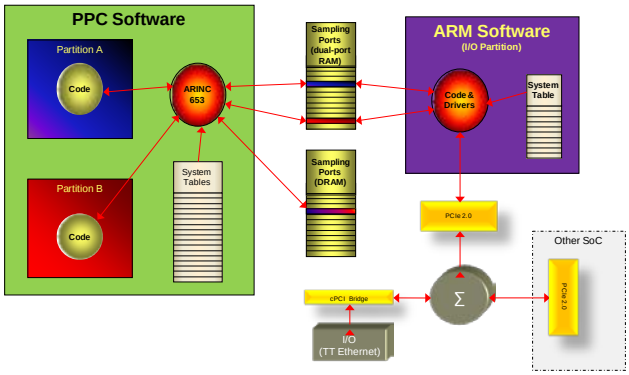

Figure 6 - Dynamic Flight Computer Software Architecture. *The software architecture is completely abstracted from the hardware and implements ARINC 653 partitions that are backward compatible to prior generations.*

To demonstrate the viability of this SoC concept, Honeywell is implementing a demonstration system using the Vertex V5 FPGA. This concept will be deployed at the end of 3Q11 and is shown in Figure 7.

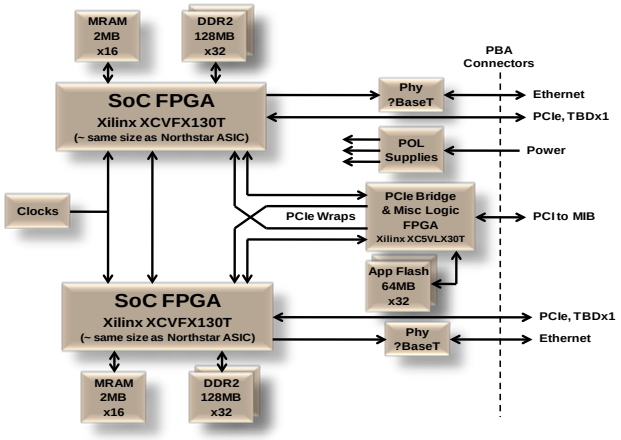

Figure 7 - Dynamic Flight Control Computer SoC based Self-Checking Pair Demonstration.

Type 2 Implementation

The implementation of the Attitude Control System SoC (Type 2) followed most of the current Honeywell architectures. The system is enhanced with vector processor accelerators to provide the necessary computational power at the lowest power. The system was architected to utilize the same processing core (in a soft core IP that can be implemented in a radiation hardened technology) and interface bus. This allows test vector commonality to reduce cost and produces common development tools to further reduce costs. The Type 2 SoC concept is shown if Figure 7.

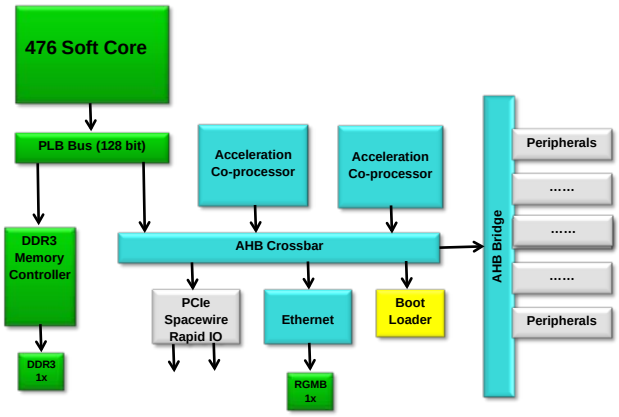

Figure 8 - Type 2 SoC Implementation Concept

Type 2 Implementation Alternative

Another alternative to a SoC processor to execute ACS satellite control implementation is to use one of the new large gate count FPGAs. Honeywell has been working with National Instruments and has created a single board device that supports the Xilinx 5QV. The scalability of existing tools will drive a step change in the ability to program these devices for this type of mission at affordable costs. This high order abstraction enables the management of complexity and therefore an increase in system complexity. This device is shown in Figure 9.

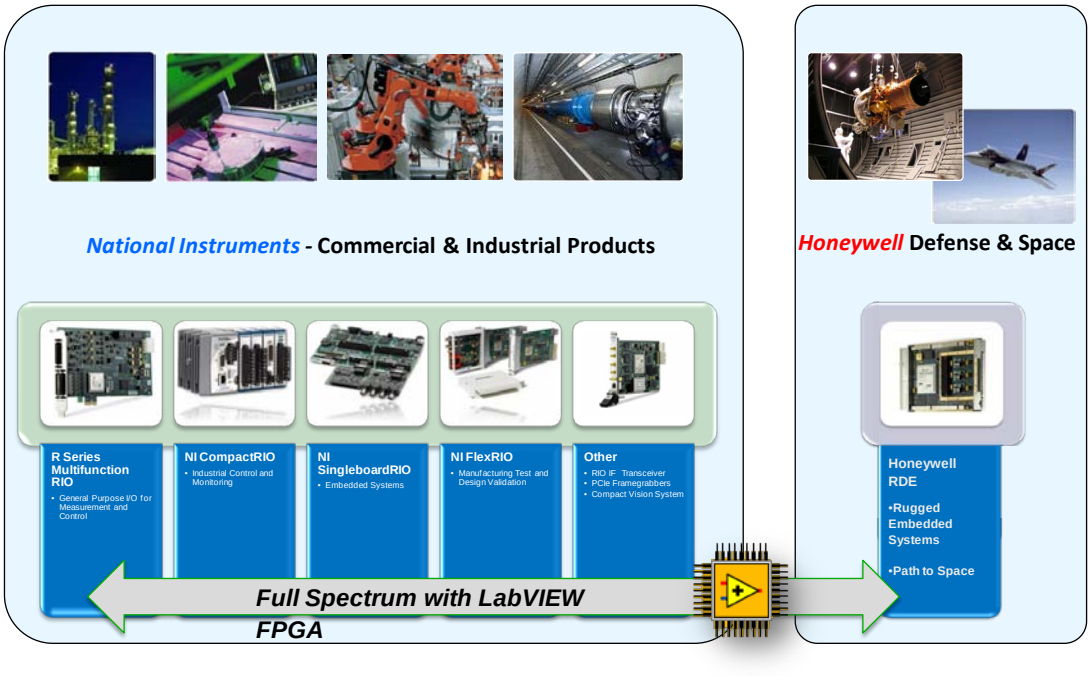

Figure 9 - Alternate Type 2 Satellite Control Processer. ***It is estimated that 50% of the functionality in future satellite systems will be instantiated in FPGAs.***

Recommendations for NASA Roadmap

The following items are suggested as enhancements to the NASA roadmaps:

1) New single core processing architectures for real-time critical & deterministic applications still have a vast improvement potential over current architectures (e.g. x10 improvement in SWaP); these improvements should be developed prior to multi-core since they will be a key at enabling efficient multi-core architectures.

2) A key challenge for multi-core is achieving deterministic operation in real-time critical applications – current COTS multi-core solutions tend to be non-deterministic.

3) Flight computing processing technology must be developed in concert with advanced concepts in a Unified Data Network (UDN) and remote data concentration. Having ultimate stand-alone processing without a matched UDN capability and remote data concentration capability will strangle the system's overall capabilities in regards to SWaP, data handling capacity, system redundancy, fault tolerance and deterministic operation.

4) Standard building-blocks for advanced processing and UDN connections are needed to create systems with a scalable level of capability and fault tolerance – all using the same architecture, tools and processes.

5) The top priorities for multi-core development need to be software related – system software for multi-core computing and eliminate the multi-core programmability gap. With the emergence this year of multi-core smart phones and the similar SWaP constraints faced by smart phone developers, we would expect an industry wide effort to close the multi-core programmability gap. Tools and techniques to wring the maximum efficiency and ease of programming will develop quickly. We would argue that the highest priority should go to ensuring that hardware exists that tracks the cell phone industry hardware hooks for managing SWaP at the application and system software levels.

6) The second highest multi-core priority would go to developing/leveraging the system software to effectively manage hardware resources in an ultra-reliable context in support of high-rel, high-availability requirements. This system software falls outside the realm of commercial interest and must therefore be of central interest to the avionics and space communities.

7) While some 11.1.1 elements are at high TRL (HyperX, currently on MISSE-7, has TRL8-9) most are lower (MAESTRO at TRL6, Rad Hard Serial RapidIO is at TRL5). Additional attention should be paid to low TRL technologies like high-speed networking that are critical to overall system architecture. Without these important infrastructure elements, it will not be possible to create a truly high performance system since data starvation will become the limiting factor.

In addition, To meet the desired NASA cost required to implement all the Exploration requirements (including technical, cost, and schedule), an advances avionics system are likely to include the following:

1. *A system that is expandable and/or re-configurable in the future*
2. *A system that uses open architecture concepts to allow flexibility within the implementation*
3. *An architecture that allows third party participation either in the development of the avionics hardware or at a future time*
4. *A low cost system throughout the lifecycle - this implies low development cost, low integration cost, and future low cost of ownership*
5. *Time & Space Partitioning and Fault Tolerant Middleware*

A team of Honeywell senior systems engineers performing the analysis of open system architectural principles concluded that the following categories are most likely to produce significant savings and should be seriously considered when designing a new system:

- Widely Used Standards
- Non-Proprietary Interfaces
- Commercially Available

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